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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,772	01/15/2002	Russel A. Martin	594728109US	5077

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PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/21/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,772	MARTIN, RUSSEL A.	
	Examiner	Art Unit	
	Jennifer T Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING (S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In the cross-reference to related application(s), the related U.S. Patent Application No. should be filed with the specific Patent Application Number.

A brief summary of the invention is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown Elliott et al. (Pub. No.: US 2003/0117423) in view of Senda et al. (Pub. No.: US 2002/0047822 A1).

Regarding claims 1, 13, 17, 19, 20, 30, and 39, referring to Figs. 3-6, 11A and 11B, Brown Elliott teaches a pixel display circuit (20) comprising: a pixel matrix (21), the pixel matrix (21) having a first pixel (24) component corresponding to a first color (R), a second pixel (26) component corresponding to a second color (G), a third pixel (22) component corresponding to a third color (B), a fourth pixel (24) component corresponding to the first color (R), and a fifth pixel (26) component corresponding to the second color (G), each of the pixel components being coupled to a charge storage device (i.e., sample/hold capacitor) and an associated switching device (i.e., transistor) to control activation of each selection of the pixel components (paragraphs [0040], [0041], and [0044]-[0045]).

Brown Elliott differs from claims 1, 13, 17, 19, 20, 30, and 39 in that he does not specifically teach each charge storage device receiving a pulse from a previous line prior to

activation of the associated switching device. However, referring to Fig. 1, 12, 15, 16, 17A, and 17C, Senda teaches each charge storage device (C1-C4) receiving a pulse from a previous line (GL) prior to activation of the associated switching device (Tr1-Tr4) (paragraphs [0196], [0197], [0213], and [0214]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the each charge storage device receiving a pulse from a previous line prior to activation of the associated switching device as taught by Senda in the system of Brown Elliott in order to prevent leakage current occur through the source and drain of the transistors and eliminate the image artifacts present.

Regarding claims 2 and 3, the combination of Brown Elliott and Senda teaches the switch further comprises a thin film transistor (TFT) (paragraph [0150] of Senda).

Regarding claims 4 and 5, the combination of Brown Elliott and Senda teaches the charge storage device comprises a thin film capacitor (paragraph [0150] of Senda).

Regarding claim 6, Brown Elliott further teaches the first color appears substantially red, the second color appears substantially green and the third color appears substantially blue (paragraphs [0040], [0041], and [0044]-[0045]).

Regarding claim 7, the combination of Brown Elliott and Senda teaches the each charge storage device (16) is fully charged prior to activation of the associated switching device (15) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claim 8, the combination of Brown Elliott and Senda teaches the pixel display circuit is coupled to a computing device (paragraphs [0033] and [0283] of Senda).

Regarding claims 9 and 10, the combination of Brown Elliott and Senda teaches the pixel display circuit is coupled to a video signal and a television signal (paragraphs [0033] and [0283] of Senda).

Regarding claims 11 and 12, Brown Elliott further teaches the pixel display circuit is coupled to a thin film emissive display device and to a LCD display device (paragraph [0065]).

Regarding claims 14, 18, 21, 31, and 40, the combination of Brown Elliott and Senda teaches the first control signal (GL) causes a voltage to be applied to one electrode of the capacitor (C1-C4) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claims 15, 22, 32, and 41, the combination of Brown Elliott and Senda teaches the second control signal (GL) causes the switch (Tr1-Tr4) to change an optical output associated with the subpixel element (M1-M4) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claims 16, 23, 24, 33, and 42, Brown Elliott further teaches the plurality of pixels (22, 24, and 26) form an array and wherein each pixel (24) of the array is coupled to a gate line (50) and a data line (40) such that control signals are transmitted to each switch (52) via the gate line (50), and wherein the capacitor (i.e., hold capacitor circuit) is coupled to a gate line (50) associated with another pixel (26) (paragraphs [0040], [0041], and [0044]-[0045]).

Regarding claims 25 and 34, referring to Figs. 3-6, 11A and 11B, Brown Elliott teaches an LCD pixel display having a plurality of pixels (21), each of the pixels (21) of the plurality of pixel having a plurality of subpixel elements (22, 24, and 26) (paragraphs [0040], [0041], and [0044]-[0045]).

Brown Elliott differs from claims 25 and 34 in that he does not specifically teach the LCD display being controlled substantially according to a clock signal, comprising the steps of:

charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period; activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements, transmitting an optical signal from the at least one optical output at least partially in response to the data signal. However, Senda teaches the LCD display (10) being controlled substantially according to a clock signal, comprising the steps of: charging a capacitor (C1) with a first control signal (GL) during a first clock period, the first clock period occurring substantially immediately before a second clock period; activating a transistor (Tr1) with a second control signal (GL) during the second clock period, the transistor (Tr1) being electrically coupled to the capacitor (C1), and the transistor (Tr1) being coupled to at least one of the plurality of subpixel elements (M1), the transistor (Tr1) coupling a data signal (SL) in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements (M1-M4), transmitting an optical signal from the at least one optical output at least partially in response to the data signal (SL) (paragraphs [0149], [0150], [0196], [0197], [0213], and [0214]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the LCD display being controlled substantially according to a clock signal, comprising the steps of: charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period; activating a transistor with a second control signal during the second clock period, the transistor

being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements, transmitting an optical signal from the at least one optical output at least partially in response to the data signal as taught by Senda in the system of Brown Elliott in order to prevent leakage current occur through the source and drain of the transistors and eliminate the image artifacts present.

Regarding claims 26 and 35, the combination of Brown Elliott and Senda teaches the first control signal (GL) causes a voltage to be applied across the capacitor (C1) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claims 27 and 36, the combination of Brown Elliott and Senda teaches the second control signal (GL) causes the transistor (Tr1) to create a potentially visible optical output associated with one subpixel element (M1) of the plurality of subpixel elements (M1-M4) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claims 28 and 37, the combination of Brown Elliott and Senda teaches the plurality of pixels form an array and wherein each pixel (M1) of the array is coupled to a first gate line (GL), a second gate line (GL) and a data line (SL), such that the first control signal is received from the first control line (GL) coupled to the capacitor (C1), the second control signal is received from the second control line (GL) coupled to the transistor (Tr1), and the data signal is received from the data line (SL) coupled to the transistor (Tr1) (paragraphs [0196], [0197], [0213], and [0214] of Senda).

Regarding claims 29 and 38, Brown Elliott further teaches each pixel (21) of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line (50), wherein each subpixel (22) further comprises a sample and hold circuit (paragraph [0045]).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ota et al. (U.S. Patent No. 5,854,616) teaches active matrix type LCD.

Brown Elliott et al. (Pub. No.: US 2003/0034992) teaches conversion of sub-pixel format data to another sub-pixel data format.

Brown Elliott et al. (Pub. No.: US 2003/0103058) teaches methods and systems for sub-pixel.

Yeon et al. (Pub. No.: US 2002/0118184) teaches gray voltage generation circuit.

Matsueda (Pub. No.: US 2002/0149556) teaches LCD apparatus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to: 703-872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

Jennifer T. Nguyen
11/13/2003

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600